BR32F402NS

DataSheet

Rev1.0.4

CMOS
Microcontroller Unit

Release Number	Date	Author	Summary of Changes
1.0.0	2022/09/06	BRMICRO	This version is for initial version
1.0.1	2022/09/07	BRMICRO	Update pin multiplexing information
1.0.2	2022/09/07	BRMICRO	Update introduction and signal description
1.0.3	2022/09/20	BRMICRO	Add chip package diagram and update information description table
1.0.4	2022/09/26	BRMICRO	Update POD Parameters of Package

Section 1 Introduction

Section 2 System Memory Map

Section 3 Signal Description

Section 4 Package information

Section 5 Part numbering

Appendix A I/O DC Parameters

Section 1 Introduction

1.1 Introduction

- BR32F402NS is a MCU. It is a new 32-bit general-purpose micro controller based on the ARM® Cortex®-M4 core with best cost-performance ratio in terms of enhanced processing capacity, reduced power consumption and peripheral set. This chip is operating at 400MHz frequency.
- The core features a Floating Point Unit (FPU) that accelerates single precision floating point math operations and supports all Arm single precision instructions and data types.
- It implements a full set of DSP instructions to address digital signal control markets that demand an efficient, easy-to-use blend of control and signal processing capabilities. It also provides a Memory Protection Unit (MPU) and powerful trace technology for enhanced application security and advanced debug support.
- Multiple algorithms are embedded inside the chip to deal with diverse scenarios: face recognition algorithm and palmar vein recognition algorithm.
- The temperature range is of -25^{O}C to 65^{O}C.
- Chip package is:

  QFN48L

1.2 Features

- Cache
  - On-chip, 32K Bytes ICache,32K Bytes DCache.
  - Has two AHB bus interfaces, a master and a slave interface.
  - Has a 2-way set-associative organization.
  - Has an AHB bus interface to access its programmer's model.
- Support for debug
- On-chip, 64K Bytes of static random-access memory can only be accessed by CPU(TCMSRAM)
- On-chip, 128K Bytes of static random-access memory (SRAM):
  - Single cycle byte, half-word (16-bit), and word (32-bit) reads and writes

- On-chip, 64K Bytes of static read only memory (ROM):
  - Single cycle byte, half-word (16-bit), and word (32-bit) read access.
- On-chip embedded flash (EFLASH)
  - Memory Origanization: 256K Bytes LP
  - Read of bytes, aligned halfwords (16 bits) and aligned words (32 bits)
  - Automated program and erase operation
  - Optional interrupt on command completion
  - Data Retention: 10 years under 85 degrees
  - 0.99~1.21V/1.5~1.98V dual power supplies
- CPM
  - Multiple system clock sources
  - Separate clock divider
  - Support for power saving mode
  - Module clock can be gated separately
- Programmable 32bit Interrupt timer(PIT) :
  - 32-bit counter with modulus "initial count" register
  - Selectable as free running or count down
- Watchdog timer(WDT) :
  - 16-bit counter with modulus "initial count" register
  - Pause option for low-power modes
- Time Counter :
  - 16-bit counter with modulus "initial count" register
  - Pause option for low-power modes
- Reset :
  - Separate reset in and reset out signals
  - Five sources of reset:

    Power-on reset

    Software reset

    Watchdog timer

    Time Counter

    Power Attack Detect Reset (Low and High Voltage Detect Reset)

  - Status flag indicates source of last reset
- DMA Controller
  - Four independently programmable DMA controller channels
  - Data transfers in 8, 16, 32 ,64bits
  - Support single transfer, Burst 4, 8,16 transfer, and burst always under a speical case.
  - Support single cycle transfer
  - Support automatic transfer mode
  - Support LLI transfer mode
  - Follow a fixed priority rule
- DMA2D
  - The Chrom-Art Accelerator™ (DMA2D) is a graphic accelerator which offers advanced bit blitting, row data copy and pixel format conversion. It supports the following functions:

    Rectangle filling with a fixed color

    Rectangle copy

    Rectangle copy with pixel format conversion

    Rectangle composition with blending and pixel format conversion.
  - Various image format coding are supported, from indirect 4bpp color mode up to 32bppdirect color. It embeds dedicated memory to store color lookup tables.
  - An interrupt can be generated when an operation is complete or at a programmed watermark.
  - All the operations are fully automatized and are running independently from the CPU or the DMAs.
  - 4 operating modes: register-to-memory, memory-to-memory, memory-to-memory with pixel format conversion, and memory-to-memory with pixel format conversion and blending.
- EDMAC
  - The EDMAC is the controller which sends data from SRAM to peripheral or from peripheral to SRAM
  - Two independently programmable DMA controller channels
  - Programmable transfer total number

  - Programmable read buffer address and write buffer address
  - Multiple peripheral select
  - Support read, write and write then read transfer
- CRC coprocessor
  - Support CRC32 / CRC16 / CRC8
  - Support DMAC Data from CRC
  - Support EDMAC Data from CRC
- External interrupts supported(EPORT) :
  - Rising/falling edge select
  - Low-level sensitive
  - Ability for software generation of external interrupt event
  - Interrupt pins configurable as general-purpose I/O
- I2C Controller
  - Supports 10 bit addressing.
  - Supports Standard Mode, Fast Mode and High-Speed Mode
  - Software option to select between High-Speed mode and Standard/Fast mode
  - Compatibility with standard and fast-mode of I2C bus version 2.1 standard.
  - Multiple-master operation.
  - Software-programmable for one of 64 different serial clock frequencies.
  - Software-selectable acknowledge bit.
  - Interrupt-driven, byte-by-byte data transfer.
  - Arbitration-lost interrupt with automatic mode switching from master to slave.
  - Transfer completion and read configure interrupt.
  - Start and stop signal generation/detection.
  - Repeated START signal generation.
  - Acknowledge bit generation/detection.
  - Bus-busy detection.
  - Option slave address receiving enable when system clock stop mode

  - SCL or SDA line gpio function supported
- Serial communications interface (SCI):
  - Full-duplex operation
  - 13-bit baud rate prescaler
  - Programmable 8-bit or 9-bit data format
  - Separately enabled transmitter and receiver
  - Separate receiver and transmitter CPU interrupt requests
  - Two receiver wakeup methods (idle line and address mark)
  - Receiver framing error detection
  - Hardware parity checking
  - 1/16 bit-time noise detection
  - General-purpose I/O capability
- Serial communications interface (SCI_TS):
  - Separate 16x9 transmit (TX) and receive (RX) FIFOs to reduce CPU interrupt service loading
  - FIFO trigger levels of 1/8, 1/4, 1/2, 3/4, and 7/8
  - Automatic hardware flow control supported
  - Serial IR interface low-speed,IrDA-compatible(up to 115.2Kbit/s)
  - Full-duplex operation
  - 13-bit baud rate prescaler
  - Programmable 8-bit or 9-bit data format
  - Separately enabled transmitter and receiver
  - Separate receiver and transmitter CPU interrupt requests
  - Two receiver wakeup methods (idle line and address mark)
  - Receiver framing error detection
  - Hardware parity checking
  - 1/16 bit-time noise detection
  - General-purpose I/O capability
- USBOTG 2.0
  - Supports internal reference clock or external 12MHz crystal reference clock

  - Performs all transaction scheduling in hardware
  - Operates either as a function controller for a USB peripheral or as the host/peripheral in point-to-point communications with another USB function
  - Synchronous RAM interface for FIFOs
  - Supports point-to-point communications with one high-speed device
  - Supports Session Request Protocol (SRP) and Host Negotiation Protocol (HNP)
  - Supports Suspend and Resume
  - Configurable for up to 15 additional Transmit endpoints and up to 15 additional Receive endpoints
  - Configurable FIFOs, including the option of dynamic FIFO sizing
  - Support for DMA access to FIFOs
- Soft connect/disconnect option PWM
  - Programmable period
  - Programmable duty cycle
  - Two Dead-Zone generator
  - Capture function
  - Pins can be configured as general-purpose I/O
- PWMT
  - 16-bit up, down, up/down auto-reload counter
  - 16-bit programmable prescaler allowing dividing (also “on the fly”) the counter clock frequency either by any factor between 1 and 65536
  - Up to 4 independent channels
  - Complementary outputs with programmable dead-time
  - Synchronization circuit to control the timer with external signals and to interconnect several timers together
  - Repetition counter to update the timer registers only after a given number of cycles of the counter
  - Interrupt/DMA generation on the some events
- Controller Area Network (CAN):
  - Full implementation of the CAN protocol specification, version 2.0B
  - Flexible Message Buffers (up to 64) of zero to eight bytes data length

  - Programmable loop-back mode supporting self-test operation
  - Time Stamp based on 16-bit free-running timer
  - Global network time, synchronized by a specific message
  - Maskable interrupts
- ADC
  - 12-bit, 10-bit, 8-bit or 6-bit configurable resolution
  - ADC conversion time: 1.0 μs for 12-bit resolution (1 MHz), 0.88 μs conversion time for 10 bit resolution, faster conversion times can be obtained by lowering resolution.
  - Programmable sampling time
- MIPI
  - The MIPI CSI-2 Host Controller supports the following features:
  - Compliant with MIPI Alliance Standard for Camera Serial Interface 2 (CSI-2),Version 1.00 - 29 November 2005
  - Interface with MIPI D-PHY following PHY Protocol Interface (PPI), as
  - defined in MIPI Alliance Specification for D-PHY, Version 1.00.00 - 14 May 2009
  - Supports up to 4 D-PHY Rx Data Lanes
  - Dynamically configurable multi-lane merging
  - Long and Short packet decoding
  - Timing accurate signaling of Frame and Line synchronization packets
  - Support for several frame formats such as:
  - General Frame or Digital Interlaced Video with or without accurate sync timing
  - Data type (Packet or Frame level) and Virtual Channel interleaving
  - 32-bit Image Data Interface delivering data formatted as recommended in CSI-2 Specification;
  - Supports all primary and secondary data formats:
  - RGB, YUV and RAW color space definitions
  - From 24-bit down to 6-bit per pixel
  - Generic or user-defined byte-based data types
  - Error detection and correction:

  - PHY level
  - Packet level
  - Line level
  - Frame level
- Secure features
  - Internal power on reset
  - Voltage detector
  - Ligth detector
  - Power Glitch detector
  - Metal Shield protection
  - Temperature detector
  - Data encryption
  - Clock and reset pulse filtration
  - Safe optimized routing
- Crypto Accelerator module
  - Large operand size N integer arithmetic

    32 * R bits

    R is positive integer from 1 to 64
  - Programmable scalar or modulo operation

    Y = (A * B) mod M

    $Y = (A^E) \bmod M$
  - Discrete "sea-of-gates" implementation to protection against SPA and probing attacks
- AES module
  - Support AES encryption/decryption algorithm
  - Support AES algorithm with 128/192/256 bits key
  - Support Electronic Code Book (ECB) mode operation and CTR(counter) mode operation
- SHA coprocessor
  - SM3(256)
  - SHA-0(160)

  - SHA-1(160)
  - SHA-224(224)
  - SHA-256(256)
  - SHA-384(384)
  - SHA-512(512)
  - Share hardware between different SHA processing
- SM4 module
  - Support sm4 encryption/decryption algorithm.
  - Support sm4 algorithm with 128 bits key
  - Support ECB and CBC mode
  - Support MLBBUS Interface
- DES coprocessor
  - Support DES and Triple-DES encryption and decryption algorithm
  - Support DES algorithm with 64(56) bits key
  - Support Triple-DES algorithm with 128(112) bits or 192(168) bits key
  - Support ECB mode and CBC mode
  - Support MLBBUS Interface
- TRNG(random number generator)
  - Max Rate: 20Mbps
- PXLP
  - Single AHB master bus architecture
  - User programmable offset for sources and destination areas of picture for dma
  - User programmable sources and destination addresses on the whole memory space
  - Copy from an area to another
  - Support average filter algorithm
  - Support histogram algorithm
  - Support hough algorithm
  - Support Reed-Solomon(RS) error correction algorithm
  - Support binary image

  - Support look for Minmum value,Maxmum value and computing average value in the block(Min_MAX_Average, MMA),The image split number of blocks is no more than 32. Support user programmable the block size.
  - Look for Minmum value,Maxmum value and computing average value in the block(Min_MAX_Average, MMA), support the image data from Digital Camera Interface (DCMI) directly.
  - Support black white run length coding algorithm
  - Interrupt generation on process completion
  - Support YOLO v3 deep learning end-to-end real-time target detection algorithm
  - Darknet light open source deep learning framework realized by YOLO v3, with less dependence and good portability. Due to its outstanding ability of speed and precision, especially small object detection, Darknet is widely used at present
- DCMI
  - 8-bit parallel interface(DVP)
  - Embedded/external line and frame synchronization
  - Continuous or snapshot mode
  - Crop feature
  - Supports the following data formats:
  - 8- bit progressive video: either monochrome or raw bayer
  - YCbCr 4:2:2 progressive video and gray output
  - YCbCr 4:2:0 directly output and gray output
  - RGB 565 progressive video and gray output
  - Supports internal DMA and external DMA for RGB and gray data output simultaneously
  - Supports internal DMA and external DMA exchangable
  - Supports MIPI-IPI format
  - Supports Crop for gray window
- SSI
  - Serial-master operation
  - DMA controller interface – Enables the SSI to interface to a DMA controller over the bus using handshaking interface for transfer requests.
  - Clock stretching support in enhanced SPI transfers

  - Data item size (4 to 32 bits) – Item size of each data transfer under control of the programmer
  - FIFO depth – Configurable depth of the transmit and receive FIFO buffers from 2 to 256 words deep. The FIFO width is fixed at 32 bits
  - Enhanced SPI support
  - Execute in Place (XIP) mode support
- PCI
  - VD detect voltage of button cell and chip output voltage.
  - NVSRAM 32x32bit
  - SDIO 8 bit detect
  - Async Timer
- GPIO
  - Support 26 GPIO

1.3 Block Diagram

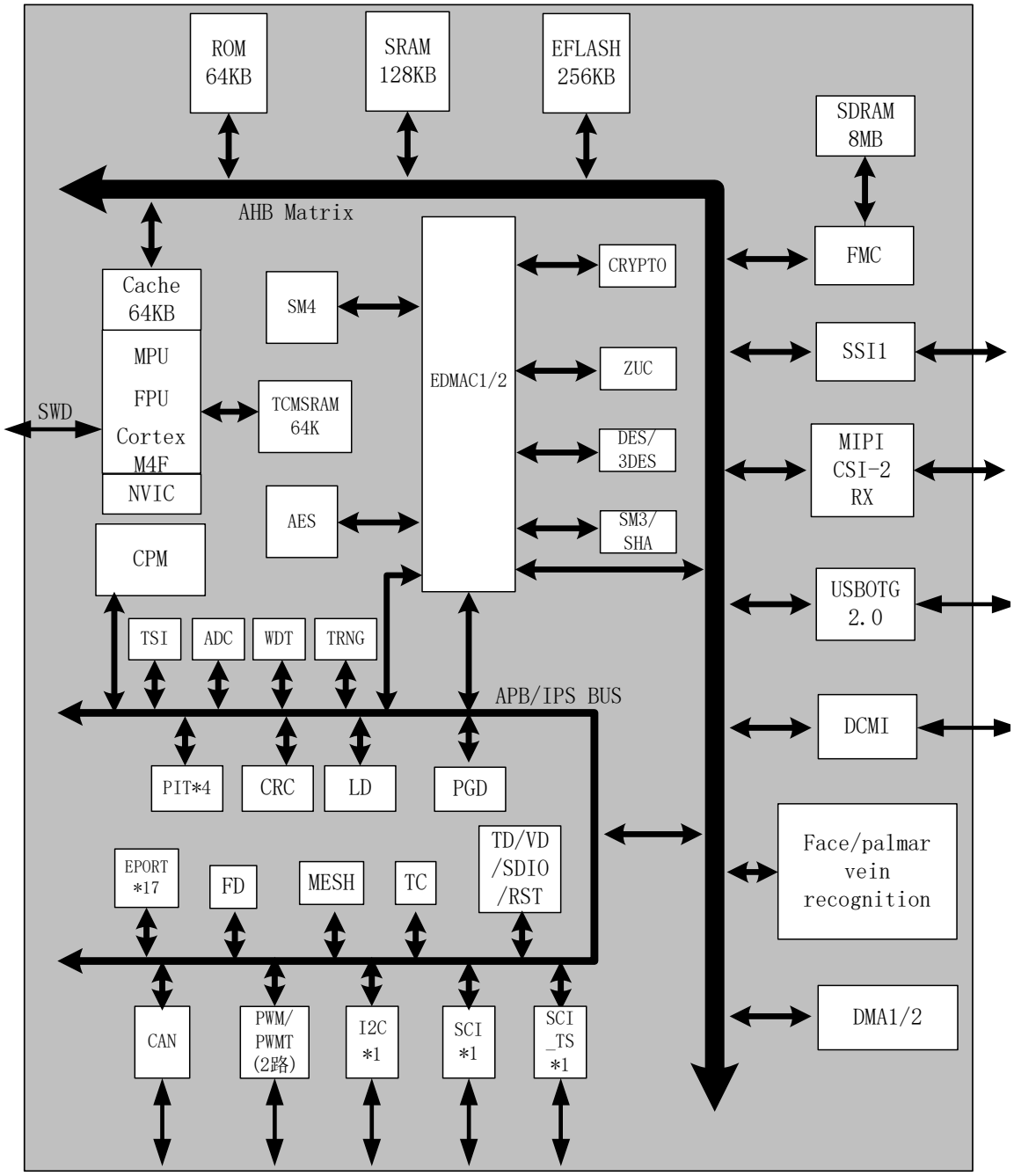


Figure 1-1 Block Diagram

Section 2 System Memory Map

2.1 Introduction

The address map, shown in **2.2**, includes:

- 64K Bytes of internal read only memory (ROM)
- 128K Bytes of internal static random-access memory (SRAM)
- 64K Bytes TCMSRAM
- 256K Bytes EFLASH
- 8M Bytes SDRAM
- Internal memory mapped registers
- Memory suppout power failure protection

2.2 Address Map

Table 2-1 Boot Modes

mode[1]	mode[0]	Boot mode	Aliasing
0	0	ROM	ROM is selected as the boot space
0	1	EFLASH	EFLASH is selected as the boot space
1	0	SDRAM	SDRAM is selected as the boot space

Table 2-2 Memory mapping vs Boot mode/physical remap

Address	Boot/Remap in ROM	Boot/Remap in EFLASH	Boot/Remap in SDRAM	Boot/Remap in SPI FLASH
0xA4000000~ 0xA7FFFFFF	SDRAM2LCD	SDRAM2LCD	SDRAM2LCD	SDRAM2LCD
0x80000000~ 0x87FFFFFF	SDRAM	SDRAM	SDRAM	SDRAM
0x20000000~ 0x2001FFFF	SRAM	SRAM	SRAM	SRAM
0x1FFF0000~ 0x1FFFFFFF	TCMSRAM	TCMSRAM	TCMSRAM	TCMSRAM
0x18000000~ 0x1BFFFFFF	SDRAM (Cached)	SDRAM (Cached)	SDRAM (Cached)	SDRAM (Cached)

Table 2-2 Memory mapping vs Boot mode/physical remap

0x14000000~ 0x17FFFFFF	SPI2 FLASH (Cached)	SPI2 FLASH (Cached)	SPI2 FLASH (Cached)	SPI2 FLASH (Cached)
0x10000000~ 0x13FFFFFF	SPI1 FLASH (Cached)	SPI1 FLASH (Cached)	SPI1 FLASH (Cached)	SPI1 FLASH (Cached)
0x08000000~ 0x0803FFFF	EFLASH	EFLASH	EFLASH	EFLASH
0x04000000~ 0x0400FFFF	ROM	ROM	ROM	ROM
0x00000000~ 0x03FFFFFF	ROM(64K) Aliased	EFLASH(256K) Aliased	SDRAM(16M) Aliased	SSI1(64M) Aliased

Table 2-3 Register Address Location Map

0x4000_0000	4Kbyte	AHB_IPS1	IO Control Module(IOCTRL)
0x4000_1000	4Kbyte		Chip configuration (CCM)
0x4000_2000	4Kbyte		Reset (RESET)
0x4000_3000	4Kbyte		TFM
0x4000_4000	4Kbyte		CPM
0x4000_5000	4Kbyte		Watchdog timer (WDT)
0x4000_6000	4Kbyte		TC
0x4000_7000	4Kbyte		PIT1
0x4000_8000	4Kbyte		PIT2
0x4000_9000	4Kbyte		Edge Port 16(EPORT16)
0x4000_a000	4Kbyte		EDMAC1
0x4000_b000	4Kbyte		Edge Port 14(EPORT14)
0x4000_c000	4Kbyte		Edge Port 15(EPORT15)
0x4000_d000	4Kbyte		PIT3
0x4000_e000	4Kbyte		PIT4
0x4000_f000	4Kbyte		CAN
0x4001_0000	4Kbyte		SPI1
0x4001_1000	4Kbyte		SPI2
0x4001_2000	4Kbyte		SPI3
0x4001_3000	4Kbyte		SCI1
0x4001_4000	4Kbyte		SCI2
0x4001_5000	4Kbyte		Reserved
0x4001_6000	4Kbyte		USI3
0x4001_7000	4Kbyte		I2C
0x4001_8000	4Kbyte		PWM
0x4001_9000	4Kbyte		Edge Port (EPORT)
0x4001_a000	4Kbyte		Edge Port 1(EPORT1)
0x4001_b000	4Kbyte		I2C2
0x4001_c000	4Kbyte		I2C3
0x4001_d000	4Kbyte		SCI_TS1

0x4001_e000	4Kbyte	AHB_IPS1	SCI_TS2
0x4001_f000	4Kbyte		PWMT
0x4002_0000	4Kbyte		ADC
0x4002_1000	4Kbyte		DAC
0x4002_2000	4Kbyte		MCC
0x4002_3000	4Kbyte		TSI
0x4002_4000	4Kbyte		Edge Port 2(EPORT2)
0x4002_5000	4Kbyte		Edge Port 3(EPORT3)
0x4002_6000	4Kbyte		Edge Port 4(EPORT4)
0x4002_7000	4Kbyte		Edge Port 5(EPORT5)
0x4002_8000	4Kbyte		Edge Port 6(EPORT6)
0x4002_9000	4Kbyte		Edge Port 7(EPORT7)
0x4002_a000	4Kbyte		Edge Port 8(EPORT8)
0x4002_b000	4Kbyte		Edge Port 9(EPORT9)
0x4002_c000	4Kbyte		Edge Port 10(EPORT10)
0x4002_d000	4Kbyte		Edge Port 11(EPORT11)
0x4002_e000	4Kbyte		Edge Port 12(EPORT12)
0x4002_f000	4Kbyte		Edge Port 13(EPORT13)
0x4003_0000	4Kbyte		LD
0x4003_1000	4Kbyte		True Random Number Generator (TRNG)
0x4003_2000	4Kbyte		PGD
0x4003_3000	4Kbyte		SEC_DET
0x4003_4000	4Kbyte		PCI
0x4003_5000	4Kbyte		PMU_RTC
0x4003_6000	4Kbyte	AHB_IPS2	Reserved
0x4003_7000	4Kbyte		CRYPTO
0x4003_8000	4Kbyte		SHA
0x4003_9000	4Kbyte		EDMAC0
0x4003_a000	4Kbyte		Reserved
0x4004_0000	4Kbyte	AHB1(AHB_CLB)	Data Encryption Standard Module (DES)
0x4004_1000	4Kbyte		AES
0x4004_2000	4Kbyte		SM4
0x4004_3000	4Kbyte		ZUC
0x4004_4000	4Kbyte	AHB2	CRC0
0x4004_5000	4Kbyte		CRC1
0x4004_6000	4Kbyte		DMAC1
0x4004_7000	4Kbyte		DMAC2
0x4004_8000	4Kbyte		CLCD
0x4004_9000	4Kbyte		TRNG_OSC
0x4004_a000	4Kbyte		SD_HOST

0x4004_c000	4Kbyte	AHB3	USBC
0x4005_0000	4Kbyte	AHB_APB	MIPI
0x4005_1000	4Kbyte		Cache_Config
0x4005_2000	4Kbyte		DMA2D
0x4005_3000	4Kbyte		DCMI
0x4005_4000	4Kbyte		PXLP
0x4005_5000	4Kbyte		Cache2_Config
0x4005_6000	4Kbyte		DCMI_DVP
0x4005_7000	4Kbyte		I2S
0x4006_0000	64Kbyte	AHB_MAC	MAC
0x6000_0000	4Kbyte	AHB_SSI1	SSI1
0x7000_0000	4Kbyte	AHB_SSI2	SSI2
0x9c00_0000	4Kbyte	AHB_SDRAM	SDRAM
0xa800_0000	4Kbyte	AHB_SDRAM2LCD	SDRAM2LCD
0xe000_0000	4Kbyte	M4	M4 SYS

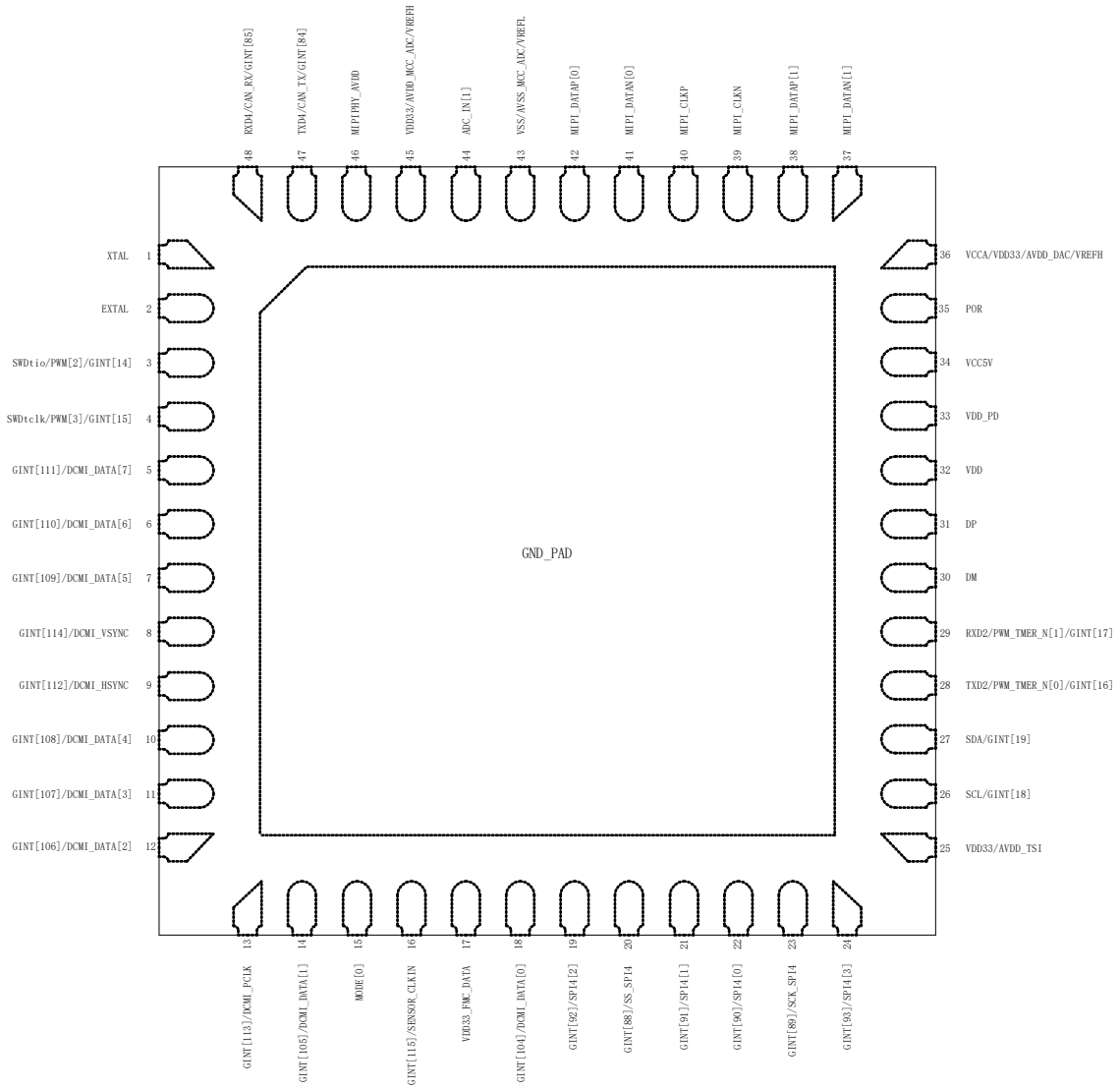
Section 3 Signal Description

3.1 Introduction

The chip is available in package:

- QFN48L(8M SDRAM)

3.2 Package Pinout Summary



3.3 Signal Properties Summary

below is the signal description.

Table 3-1 Signal Description

Pin No.	Name[1]	Alternate	Dir.	Power	Default	Pin Pull	Description
Reset(1)							
35	por	-	I	VCC5V	H	-	power down reset
Mode(1)							
15	mode[0]	-	I	VDD33	L	-	boot mode select input
Clock(2)							
1	xtal	-	O	VDD33	-	-	12MHz Oscillator clock output
2	extal	-	I	VDD33	-	-	12MHz Oscillator clock in
DCMI (12)							
5	dcmi_data[7]	GINT[111]	I/O	VDD33	H	Pullup/Pulldown	DCMI data bus
6	dcmi_data[6]	GINT[110]	I/O	VDD33	H	Pullup/Pulldown	DCMI data bus
7	dcmi_data[5]	GINT[109]	I/O	VDD33	H	Pullup/Pulldown	DCMI data bus
8	dcmi_vsync	GINT[114]	I/O	VDD33	H	Pullup/Pulldown	DCMI vertical synchronization
9	dcmi_hsync	GINT[112]	I/O	VDD33	H	Pullup/Pulldown	DCMI horizontal synchronization
10	dcmi_data[4]	GINT[108]	I/O	VDD33	H	Pullup/Pulldown	DCMI data bus
11	dcmi_data[3]	GINT[107]	I/O	VDD33	H	Pullup/Pulldown	DCMI data bus
12	dcmi_data[2]	GINT[106]	I/O	VDD33	H	Pullup/Pulldown	DCMI data bus
13	dcmi_pclk	GINT[113]	I/O	VDD33	L	Pullup/Pulldown	DCMI clock
14	dcmi_data[1]	GINT[105]	I/O	VDD33	H	Pullup/Pulldown	DCMI data bus
18	dcmi_data[0]	GINT[104]	I/O	VDD33	H	Pullup/Pulldown	DCMI data bus
16	sensor_clkin	GINT[115]	I/O	VDD33	L	Pullup/Pulldown	DCMI clock input
I2C(2)							
26	scl	GINT[18]	I/O	VDD33	L	Pullup/Pulldown	I2C clock
27	sda	GINT[19]	I/O	VDD33	L	Pullup/Pulldown	I2C data
USB(2)							
31	dp	-	I/O	VCCA	-	-	USB data
30	dm	-	I/O	VCCA	-	-	USB data
ADC(1)							
44	adc_in[1]	-	I	VDD33	-	-	adc channel input

Signal Description

Pin No.	Name[1]	Alternate	Dir.	Power	Default	Pin Pull	Description
MIPI (6)							
37	MIPI_DATAN[1]	-	I/O	MIPIPHY _AVDD	-	-	MIPI data negative
38	MIPI_DATAP[1]	-	I/O	MIPIPHY _AVDD	-	-	MIPI data positive
39	MIPI_CLKN	-	I/O	MIPIPHY _AVDD	-	-	MIPI data negative
40	MIPI_CLKP	-	I/O	MIPIPHY _AVDD	-	-	MIPI clock positive
41	MIPI_DATAN[0]	-	I/O	MIPIPHY _AVDD	-	-	MIPI data negative
42	MIPI_DATAP[0]	-	I/O	MIPIPHY _AVDD	-	-	MIPI data positive
SSI(6)							
19	spi4[2]	GINT[92]	I/O	VDD33	H	Pullup/Pulldown	SPI data
20	ss_spi4	GINT[88]	I/O	VDD33	H	Pullup/Pulldown	SPI chip select
21	spi4[1]	GINT[91]	I/O	VDD33	H	Pullup/Pulldown	SPI data bus
22	spi4[0]	GINT[90]	I/O	VDD33	H	Pullup/Pulldown	SPI data bus
23	sck_spi4	GINT[89]	I/O	VDD33	L	Pullup/Pulldown	SPI clock
24	spi4[3]	GINT[93]	I/O	VDD33	H	Pullup/Pulldown	SPI data bus
UART(4)							
28	txd2	PWM_TIMER_N[0]/ GINT[16]	I/O	VDD33	H	Pullup/Pulldown	UART transmitting data /PWM output
29	rxd2	PWM_TIMER_N[1]/ GINT[17]	I/O	VDD33	H	Pullup/Pulldown	UART receiving data /PWM output
47	txd4	CAN_TX/GINT[84]	I/O	VDD33	H	Pullup/Pulldown	UART transmitting data/ CAN transmitting data
48	rxd4	CAN_RX/GINT[85]	I/O	VDD33	H	Pullup/Pulldown	UART receiving data/ CAN recerving data
SWD(2)							
3	gint[14]	SWD_TIO/PWM[2]	I/O	VDD33	H	Pullup/Pulldown	STExternal interrupt
4	gint[15]	SWD_TCLK/PWM[3]	I/O	VDD33	H	Pullup/Pulldown	STExternal interrupt
POWER(9)							
32	VDD	-	-	-	-	-	1.1V power out

Pin No.	Name[1]	Alternate	Dir.	Power	Default	Pin Pull	Description
17	VDD33_FMC_DATA	-	-	-	-	-	3.3V power input for SDRAM DATA
25	VDD33/ AVDD_TSI	-	-	-	-	-	3.3V power for TSI
33	VDD_PD	-	-	-	-	-	1.1V power out for Core
34	VCC5V	-	-	-	-	-	3.3V power input for chip
36	VDD33/VCCA/ AVDD_DAC /VREFH	-	-	-	-	-	reference voltage for DAC
45	VDD33/AVDD_ MCC_ADC /VREFH	-	-	-	-	-	reference voltage for ADC
46	MIPIPHY_AVDD	-	-	-	-	-	3.3V power input for MIPI
43	AVSS_MCC_ADC/VSS/VREFL	-	-	-	-	-	Ground

NOTES:

1. Shaded signals are for optional bond-out for more pin count package.
2. Pins are designed for anti-leakage.
3. Default Pull is configured by Wakeup PAD Control Register of CPM module.
4.All pullups are disconnected when the signal is programmed as an output.

Section 4 Package information

4.1 General

This section provides parameters for below items:

• Package Outline Dimension (POD) of package for QFN48L

4.2 POD of Package QFN48L

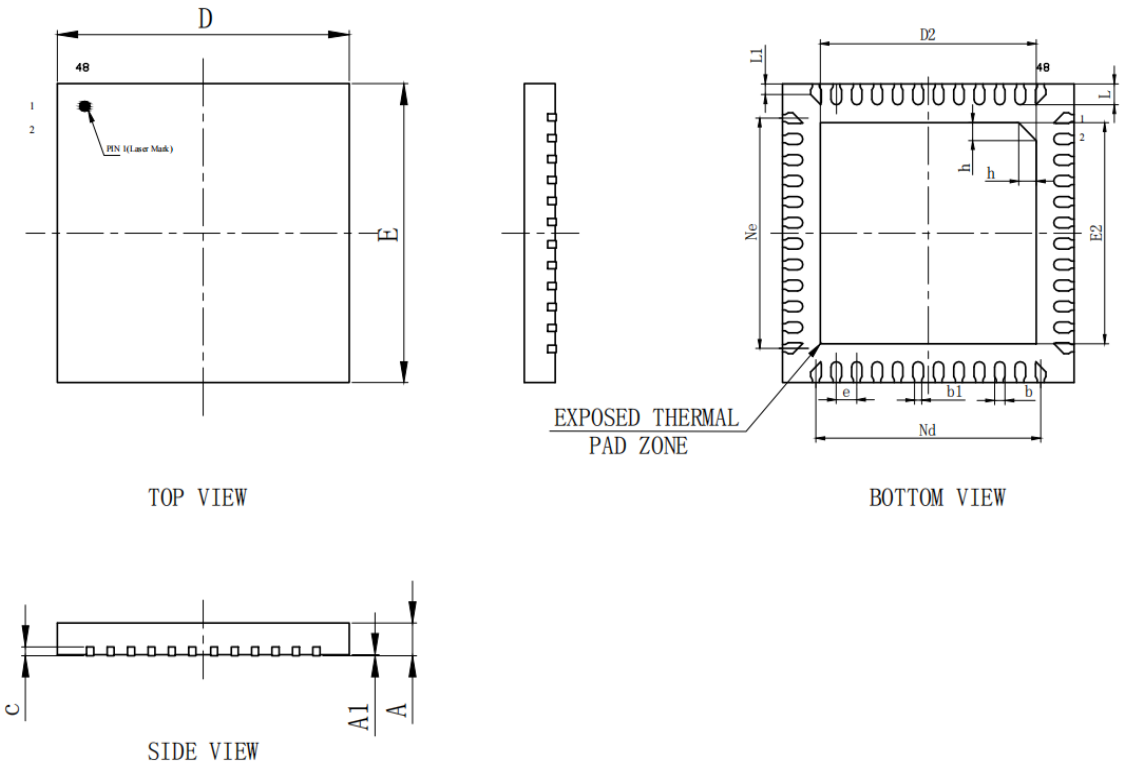


Figure 4-1 POD of Package QFN48L

Table 4-1 POD Parameters of Package QFN48L

SYMBOL	MILIMETER		
	MIN	NOM	MAX
A	0.50	0.55	0.60
	0.80	0.85	0.90
A1	0	0.02	0.05
b	0.13	0.18	0.23
b1	0.12REF		
c	0.10	0.15	0.20
D	4.90	5.00	5.10
D2	3.60	3.70	3.80
e	0.35 BSC		
Ne	3.85 BSC		
Nd	3.85 BSC		
E	4.90	5.00	5.10
E2	3.60	3.70	3.80
L	0.30	0.35	0.40
L1	0.13	0.18	0.23
h	0.25	0.30	0.35
载体尺寸（mil）	154X154		

Section 5 Part numbering

5.1 BR32F4x Series Chips Naming rules

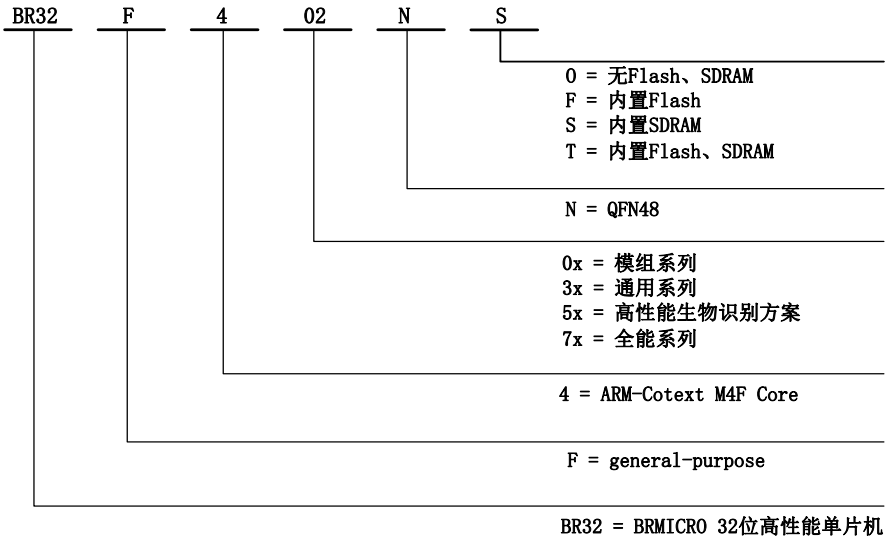


Figure 5-1 Naming rules

Appendix A I/O DC Parameters

Table 3-1 shows the DC parameters for 3.3V I/O.

Table 3-1 DC parameters,3.3V I/O

Parameter	Symbol	Test conditions	Minimum	Maximum	Units
Input HIGH Level,input, and I/O pins	V_{IH}	Guaranteed logic HIGH level	2.0	DVDD	V
Input LOW level,input, and I/O pins	V_{IL}	Guaranteed logic LOW level	VSS	0.8	V
Output HIGH voltage	V_{OH}	VDD=minimum,DVDD= minimum,I_{OH}[2]=-2mA, −4mA,−8mA,and −12mA	2.4	DVDD	V
Output LOW voltage	V_{OL}	VDD=minimum,DVDD= minimum,I_{OH}[2]=2mA, 4mA,8mA,and 12mA	VSS	0.4	V
Input pull-up resistor current	I_{RPU}	$V_{PAD}=V_{IH}$, DVDD=minimum	50[b]	-	μA
Input pull-up resistance	R_{PU}	$V_{PAD}=V_{IH}$, DVDD=minimum	9	19.4[e]	KΩ
Input pull-down resistor current	I_{RPD}	$V_{PAD}=V_{IL}$, DVDD=minimum	50[d]	-	μA
Input pull-down resistance	R_{PD}	$V_{PAD}=V_{IL}$, DVDD=minimum	6.7	16[e]	KΩ
Input hysteresis[e]	V_H		0.2[e]	-	V
Input leakage current, non-tolerant	I_{PAD}	DVDD=maximum, VPAD=0V or DVDD	-1[f]	1[f]	μA
Fail-safe Leakage Current	I_{PAD}	DVDD=0,VPAD=DVDD maximum	-	1[g]	μA
Off-State leakage current	I_{OZ}	DVDD=maximum, VPAD=0V or DVDD		1.2u[h]	μA

a. Valid only when DVDD = 2.97V,process = SS,temperature = 125℃.This current is de-rated at other PVT conditions,including typical DVDD = 1.8V and 2.5V.

b. Weak pull-up current is the minimun current flowing from DVDD to PAD when

DVDD = 2.97V,process = SS,and temperature = 125℃. This value is de-rated for all the other DVDD values.

c. The weak pull-up and pull-down resistance is the maximum resistance with the test conditions specified when DVDD = 2.97V,process = SS and temperature = 125℃.

d. Weak pull-down current is the minimum current flowing from PAD to ground, when DVDD = 2.97V,process = SS,and temperature = 125℃. This value is de-rated for all the other DVDD values.

e. Valid only when hysteresis is enabled.Simulation conditions for FF:temperature = -40℃ and DVDD = 3.63V.Simulation condition for SS:temperature = 125℃ and DVDD = 2.97V.

f. Input leakage current is the current that flows to or out of the PAD node.This leakage is measured when DVDD = 3.63V,process = FF and temperature = 125℃.

g. Fail-safe leakage is the current flowing from PAD to DVDD and ground when DVDD is powered down. This leakage is measured with PAD = 3.63V,Process = FF,Temperature = 125℃ and DVDD = 0.

h. Input leakage current is the current that flows to or out of the PAD node.This leakage is measured when DVDD = 3.63V,process = FF and temperature = 125℃.

Table 3-2 shows the DC parameters for 2.5V I/O.

Table 3-2 DC parameters,2.5V I/O

Parameter	Symbol	Test conditions	Minimum	Maximum	Units
Input HIGH Level,input, and I/O pins	V_{IH}	Guaranteed logic HIGH level	1.7	DVDD	V
Input LOW level,input, and I/O pins	V_{IL}	Guaranteed logic LOW level	VSS	0.7	V
Output HIGH voltage	V_{OH}	VDD=minimum, DVDD=minimum,I_{OH}[2]	2.0	DVDD	V
Output LOW voltage	V_{OL}	VDD=minimum, DVDD=minimum	VSS	0.4	V
Input pull-up resistor current	I_{RPU}	$V_{PAD}=V_{IH}$, DVDD=minimum	25[b]	-	μA
Input pull-up resistance	R_{PU}	$V_{PAD}=V_{IH}$, DVDD=minimum	-	22[e]	KΩ
Input pull-down resistor current	I_{RPD}	$V_{PAD}=V_{IL}$, DVDD=minimum	25[d]	-	μA
Input pull-down resistance	R_{PD}	$V_{PAD}=V_{IL}$, DVDD=minimum	-	22[e]	KΩ
Input hysteresis[e]	V_H		0.2	-	V
Input leakage current, non-tolerant	I_{PAD}	DVDD=maximum, VPAD=0V or DVDD	-1[f]	1[f]	μA
Input leakage current, fail-safe	I_{PAD}	DVDD=0,VPAD=DVDD maximum	-	1[g]	μA
Off-State leakage current	I_{OZ}	DVDD=maximum, VPAD=0V or DVDD		1[h]	μA

a. For derating values,see Table 3-4 on page 3-4.
b. Weak pull-up current is the minimum current flowing from DVDD to PAD when DVDD = 2.25V,process = SS,and temperature = 125℃.
c. The weak pull-up and pull-down resistance is the maximum resistance with the test conditions specified when DVDD = 2.25V,process = SS and temperature = 125℃.
d. Weak pull-down current is the minimum current flowing from PAD to ground, when DVDD = 2.25V,process = SS and temperature = 125℃.

e. Valid only when hysteresis is enabled.Simulation conditions for FF:temperature = -40℃ and DVDD = 2.75V.Simulation condition for SS:temperature = 125℃ and DVDD = 2.25V.

f. Input leakage current is the current that flows to or out of the PAD node.This leakage is measured when DVDD = 2.75V,process = FF and temperature = 125℃.

g. Fail-safe leakage is the current flowing from PAD to DVDD and ground when DVDD is powered down.This leakage is measured with PAD = 2.75V,Process = FF,Temperature = 125℃ and DVDD = 0.

h. Off-state leakage current includes Input leakage current and current from all supplies,DVDD,and VDD when DVDD = 2.75V,process = FF and temperature = 125℃.

Table 3-3 shows the DC parameters for 1.8V I/O

Table 3-3 DC parameters,1. 8V I/O

Parameter	Symbol	Test conditions	Minimum	Maximum	Units
Input HIGH Level,input, and I/O pins	V_{IH}	Guaranteed logic HIGH level	0.7×DVDD	DVDD	V
Input LOW level,input, and I/O pins	V_{IL}	Guaranteed logic LOW level	VSS	0.3×DVDD	V
Output HIGH voltage	V_{OH}	VDD=minimum, DVDD=min,I_{OH}[2]	0.8*DVDD	DVDD	V
Output LOW voltage	V_{OL}	VDD=minimum, DVDD=minimum	VSS	0.2*DVDD	V
Input pull-up resistor current	I_{RPU}	V_{PAD}=V_{IH}, DVDD=minimum	15[b]	-	μA
Input pull-up resistance	R_{PU}	V_{PAD}=V_{IH}, DVDD=minimum	11.2	32.4[e]	KΩ
Input pull-down resistor current	I_{RPD}	V_{PAD}=V_{IL}, DVDD=minimum	15[d]	-	μA
Input pull-down resistance	R_{PD}	V_{PAD}=V_{IL}, DVDD=minimum	9.4	32.4[e]	KΩ
Input hysteresis[e]	V_H		0.1*DVDD	-	V
Input leakage current, non-tolerant	I_{PAD}	DVDD=maximum, VPAD=0V or DVDD	-1[f]	1[f]	μA
Input leakage current, fail-safe	I_{PAD}	DVDD=0, VPAD=DVDD maximum	-	1[g]	μA
Off-State leakage current	I_{OZ}	DVDD=maximum, VPAD=0V or DVDD		1[h]	μA

a. For derating values,see Table 3-4.
b. Weak pull-up current is the minimum current flowing from DVDD to PAD when DVDD = 1.62V,process = SS,and temperature = 125℃.
c. The weak pull-up and pull-down resistance is the maximum resistance with the test conditions specified when DVDD = 1.62V,process = SS and temperature = 125℃.
d. Weak pull-down current is the minimum current flowing from PAD to ground,

when DVDD = 1.62V,process = SS and temperature = 125℃.

e. Valid only when hysteresis is enabled.Simulation conditions for FF: temperature = -40℃ and DVDD = 1.98V.Simulation condition for SS: temperature = 125℃ and DVDD = 1.62V.

f. Input leakage current is the current that flows to or out of the PAD node.This leakage is measured when DVDD = 1.98V,process = FF and temperature = 125℃.

g. Fail-safe leakage is the current flowing from PAD to DVDD and ground when DVDD is powered dowm.This leakage is measured with PAD = 1.98V,Process = FF,Temperature = 125℃ and DVDD = 0.

h. Off-state leakage current includes Input leakage current and current from all supplies,DVDD,and VDD when DVDD = 1.98V,process = FF and temperature = 125℃.

Table 3-4 shows simulated drive current at slow PVT conditions

Table 3-4 DC driver current for PBIDIR_33_33_FS_DR[a]

Drive strength	I_{OH},DVDD =3.3V	I_{OL},DVDD =3.3V	I_{OH},DVDD =2.5V	I_{OL},DVDD =2.5V	I_{OH},DVDD =1.8V	I_{OL},DVDD =1.8V	Unit
2	2.45	2.43	1.87	1.87	1.35	1.28	mA
4	4.88	4.96	3.73	3.83	2.7	2.64	mA
8	9.76	9.84	7.47	7.59	5.4	5.22	mA
12	14.6	14.7	11.18	11.36	8.1	7.84	mA

a. PVT comers that are used for simulation:
3.3V SS/2.97V/125℃.
2.5V SS/2.25V/125℃.
1.8V SS/1.62V/125℃.
In 3.3V,IOH,and IOL measured with VDS=0.4V.

Appendix B Preliminary Electrical Characteristic

0.1 General

This section provides electrical parametrics and electrical ratings for the microcontroller unit.

0.2 Absolute Maximum Ratings

Maximum ratings are the extreme limits to which the Chip can be exposed without permanently damaging it. See **Table 0-1**.

The Chip contains circuitry to protect the inputs against damage from high static voltages; however, do not apply voltages higher than those shown in the table. Connect unused inputs to the appropriate voltage level, V_{DDH}. This device is not guaranteed to operate properly at the maximum ratings. Refer to **0.4**, **0.4**,**Table 0-3**,**Table 0-4** for guaranteed operating conditions.

Table 0-1 Absolute Maximum Ratings

Num	Rating	Symbol	Value	Unit
1	Operating temperature range	T_{OPT}	—	^{O}C
2	Storage temperature range	T_{STG}	-40 to +125	^{O}C

0.3 Electrostatic Discharge (ESD) Protection

Table 0-2 ESD Protection Characteristics

Parameter[1,2,3,4,5]	Symbol	Value	Units
ESD target for human body model	HBM	2000	V
Latch Up	Latch UP	200	mA

NOTES:

1. This report will be invalid if reproduced in whole or in part.
2. This report refers only to the specimen(s) submitted to test, and is invalid if used separately.
3. This report is ONLY valid with the examination seal and signature of this institute.
4. The tested specimen(s) will only be preserved for thirty days from the date issued, if not collected by the applicant.
5. The failure criteria of all ESD tests should be based on the result of parametric and functional testing conducted by the customer, which follows the statement of international standards. Thus, the judgment of the curve traces provided in this report is for reference ONLY.

0.4 DC Electrical Specifications

Table 0-3 DC Electrical Specificatios(3.3V)

Parameter	Symbol	Min	Typical	Max	Unit
Supply Voltage	V_{DDH}	3	3.3	3.6	V
Input High Voltage	V_{IH}	2	—	DVDD	V
Input Low Voltage	V_{IL}	VSS	—	0.8	V
Output High Voltage	V_{OH}	2.4	—	DVDD	V
Output Low Voltage	V_{OL}	VSS	—	0.4	V
Pull-up Resistor current	R_{PU}	50	—	—	υA
Input Leakage Current@DVDD=max,VPAD-0 o DVDD	I_{IN}	-1.2	—	1.2	υA
Fail leakagecurrent @DVDD=0,VPAD=DVDD=max	I_{PAD}	—	—	1.2	υA
Off_state leakage current@DVDD=max,VPAD=0 or DVDD	I_{OZ}	—	—	1.2	uA

0.5 Power Consumption

Table 0-4 power consumption[1]

Parameter	power consumption
	400MHz
CPU run	—
CPU and peripherals run[1]	—
CPU and SDRAM run[2]	—
CPU,SDRAM and peripherals run	—
LOWPOWER MODE[3]	—
POWEROFF1.0 MODE[4]	—
POWEROFF2.0 MODE[5]	—

NOTES:

1. All the peripherals are operated in fastest speed.
2. CPU:SDRAM=4:1 in speed.
3. Chip poweron and clock stop.

wakeup source: USI,I2C,EPORT,USB RESUME,TSI TOUCH,TIME COUNTER, RTC,WK PAD,USBDET,POR,PCI

4. Only TSI run in poweroff 1.0 mode.

wakeup source: EPORT0,TSI TOUCH,RTC,WK PAD,USBDET,POR,PCI

5. Only PCI poweron.

wakeup source: WK PAD,USBDET,POR

NOTES:

1. All the data are typical results.

0.6 AC Timing

0.6.1 SPI Interface

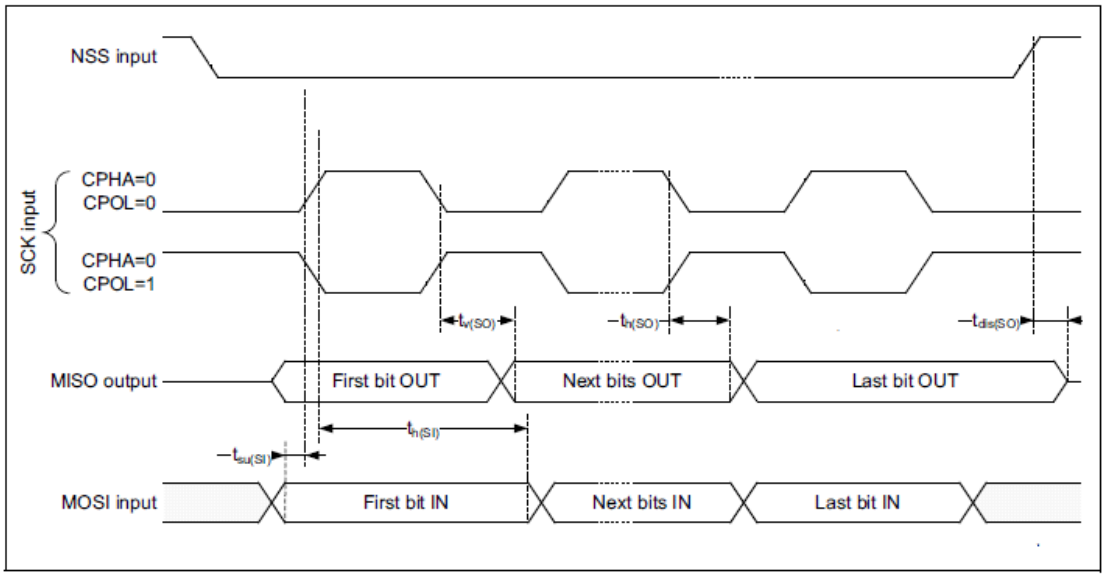


Figure 0-1 SPI timing diagram

Table 0-5 SPI characteristics

Symbol	Parameter	condition	min	typ	max	Unit
f_{sck}	SPI clock frequency	VCC3.3V,VDD 1.1V	-	-	50	MHz
		VCC3.3V,VDD 1.23V	-	-	62.5	
$t_{su(SI)}$	Data input setup time	VCC3.3V,VDD1.1V	-	3.9	6.9	ns
$t_{h(SI)}$	Data input hold time	VCC3.3V,VDD1.1V	-1	0	-	
$t_{dis(SO)}$	Data output disable time	VCC3.3V,VDD1.1V	5.9	8	11.9	
$t_{v(SO)}$	Data output valid time	VCC3.3V,VDD1.1V	-	9.8	14.95	
$t_{h(SO)}$	Data output hold time	VCC3.3V,VDD1.1V	2.3	3.9	-	

0.6.2 SSI(QSPI) Interface

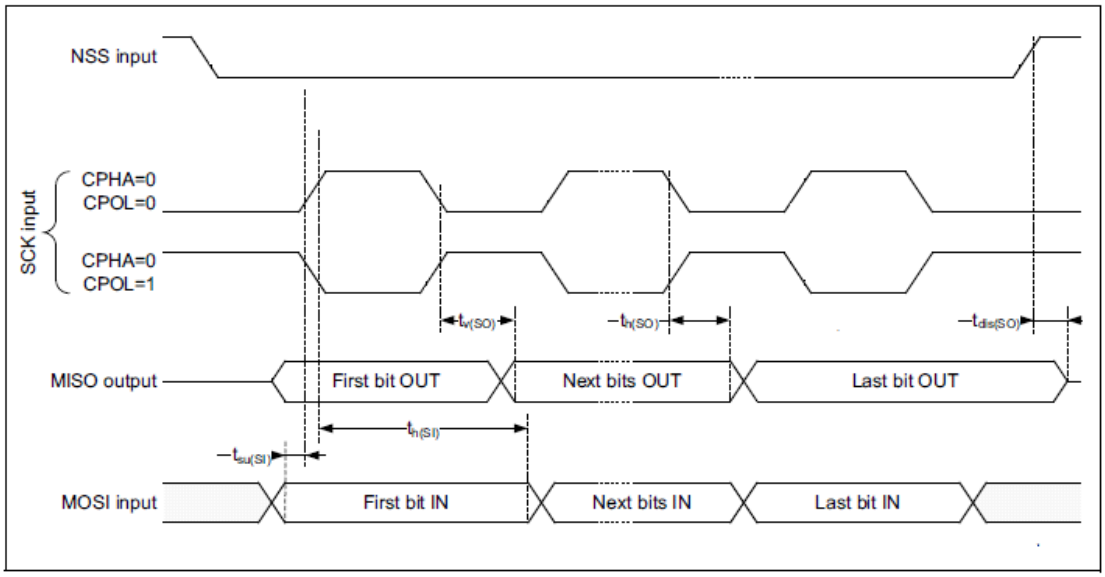


Figure 0-2 SSI(QSPI) timing diagram

Table 0-6 SSI(QSPI) characteristics

Symbol	Parameter	condition	min	typ	max	Unit
f_{sck}	SSI clock frequency	VCC3.3V,VDD 1.1V	-	-	100	MHz
		VCC3.3V,VDD 1.23V	-	-	125	
$t_{su(SI)}$	Data input setup time	VCC3.3V,VDD1.1V	2	-	-	ns
$t_{h(SI)}$	Data input hold time	VCC3.3V,VDD1.1V	3	-	-	
$t_{dis(SO)}$	Data output disable time	VCC3.3V,VDD1.1V	-	-	7	
$t_{v(SO)}$	Data output valid time	VCC3.3V,VDD1.1V	-	-	6	
$t_{h(SO)}$	Data output hold time	VCC3.3V,VDD1.1V	0	-	-	